

10/693,468

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application / Conf. No.	Unknown 10 / 693,468
				Filing Date	October 24, 2003
				First Named Inventor	Kevin T. Look
				Art Unit	Unknown 2818
				Examiner Name	Unknown V. Nguyen
				Attorney Docket Number	X-719-ID-2D US
Sheet	1	of	2		

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FOREIGN PATENT DOCUMENTS						
Examiner Initials *	Cite No.¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T *
		Country Code ² -Number ³ -Kind Code ⁴ (if known)				
		JP 40623289 A	08-01-94	Kou		
		JP 360009160 A	01-18-85	Fukumoto et al.		
		JP 408264660 A	10-11-96	Yamamoto		
		JP 2000077356 A	03-14-00	Sheen		
		JP 406232389 A	08-19-94	Kou		
		JP 363079377 A	04-09-88	Kita		
		JP 406163906 A	06-10-94	Natsume		

Examiner Signature	V. Nguyen	Date Considered	7/26/09
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Sheet 2 of 2	Attorney Docket Number	X-719-ID-2D US	

OTHER -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
W		"Boron Diffusion And Penetration In Ultrathin Oxide With Poly-Si Gate"; Cao et al.; IEEE Electron Device Letters; Vol. 19; No. 8; August 1998; pp. 291-293	
W		"Flat-band Voltage Shifts In P-MOS Devices Caused By Carrier Activation In P+-Polycrystalline Silicon and Boron Penetration"; Aoyama et al.; 1997 IEEE; pp. 26.1.1 - 26.1.4	
W		"A PROM Element Based On Salicide Agglomeration Of Poly Fuses In A CMOS Logic Process"; Alavi et al.; 1997 IEEE; pp. 34.3.1 - 34.3.4	
W		"Effects Of Thermal Processes After Silicidation On The Performance Of TiSi ₂ /Polysilicon Gate Device"; Jang et al.; IEEE Transactions On Electron Devices; Vol. 46; No. 12; December 1999; pp. 2353-2356	
W		"Comparison Of Transformation To Low-Resistivity Phase And Agglomeration Of TiSi ₂ and CoSi ₂ "; Lasky et al.; IEEE Transaction On Electron Devices; Vol. 38; No. 2; February 1991; pp. 262-269	
W		"CoSi ₂ Integrated Fuses On Poly Silicon For Low Voltage 0.18 um CMOS Application"; Kalnitsky et al.; 1999 IEEE; 4 pages	

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